2811

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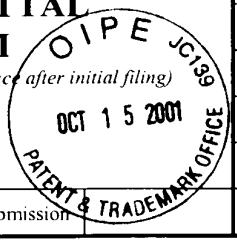

Application Number	09/433,705
Filing Date	November 4, 1999
First Named Inventor	Shunpei YAMAZAKI
Group Art Unit	2811
Examiner Name	S. Loke
Total Number of Pages in This Submission	Attorney Docket Number: 0756-2062

ENCLOSURES *(check all that apply)*

- ☐ Fee Transmittal Form
  - ☐ Fee Attached
- ☒ Amendment / Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☒ Information Disclosure Statement and Notification of Related Application
- ☐ Certified Copy of Priority Document(s)
- ☐ Response to Missing Parts/ Incomplete Application
  - ☐ Response to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Assignment Papers *(for an Application)*
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Remarks

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Firm or Individual name	Eric J. Robinson, Reg. No. 38,285 Nixon Peabody LLP 8180 Greensboro Drive Suite 800 McLean, VA 22012
Signature	
Date	October 15, 2001

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	)
Shunpei YAMAZAKI	) Group Art Unit: 2811
Serial No. 09/433,705	) Examiner: S. Loke
Filed: November 4, 1999	)
For: METHOD OF FABRICATING	)
A SEMICONDUCTOR DEVICE	)

AMENDMENT AND RESPONSE TO NON-COMPLIANT AMENDMENT

Honorable Commissioner for Patents
Washington, D.C. 20231

Sir:

In response to the *Notice of Non-Compliant Amendment* of September 13, 2001, please amend the subject application as follows:

IN THE CLAIMS:

Subt C2

Please amend claim 13.

13. (Amended) A semiconductor device comprising:

a first thin film transistor comprising:

a semiconductor island on an insulating surface;

a channel region in the semiconductor island;

B1

at least an LDD region being contact with the channel region and including a first impurity region and a second impurity region, said first impurity region being in contact with the channel region and said second impurity region being in contact with the first impurity region;

at least a third impurity region being in contact with the second impurity region; a gate electrode being formed over the semiconductor island with a gate insulating

film interposed therebetween and having a first gate electrode and a second electrode being formed on the first gate electrode,

wherein the first gate electrode has at least a taper portion and a flat portion,

wherein the first impurity region is overlapped with the taper portion of the first gate electrode with the gate insulating film interposed therebetween,